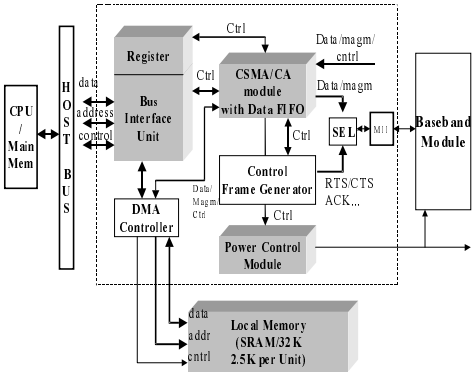
4. Design and Implementation

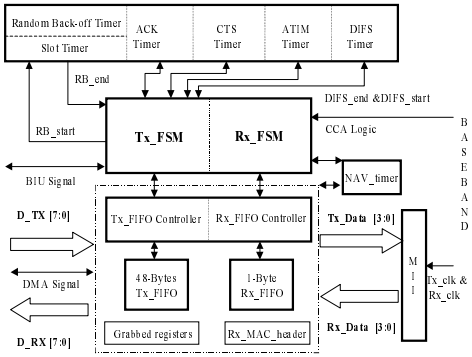


- *44MHz* System clock
- Transmission and Reception clocks are *250K* and *500KHz* for 1 Mbps and 2 Mbps data rate respectively.
- Baseband interface employs 4-bit wide MII bus.
- Host interface complies with *8-bit* PCMCIA data bus.
- Interfacing SRAM with *15-bit* address decoder and *8-bit* data bus

Software Issues

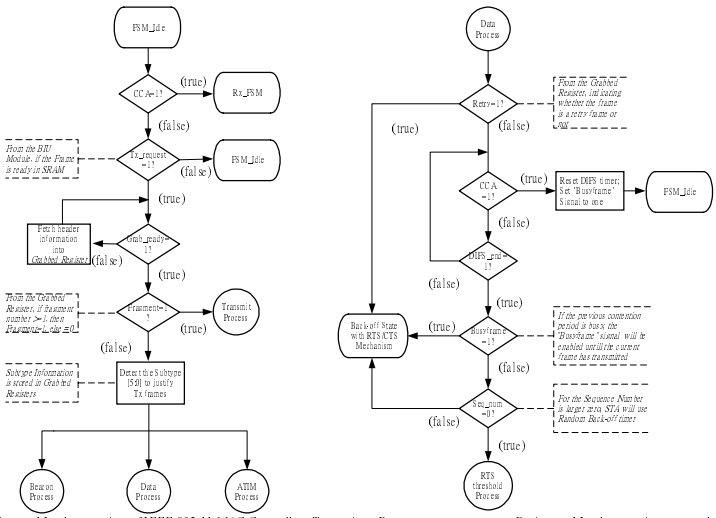
- Information exchanged between Host and MAC controller
  - The length information is added in front of the received frames before storing into the SRAM.
  - Host should fill out the Data&Management bits and Length registers to inform the MAC controller the type (data frame or management frame) and length of the current downloading frame.
    - In the current design, host should also calculate CRC16 of the PLCP header.
- Timers
  - TSF Timer
  - Beacon Timer
  - » Min&Max Probe Response Timer
  - » MAX MSDU Timer for transmission and reception

(1) CSMA/CA Module with Data FIFO

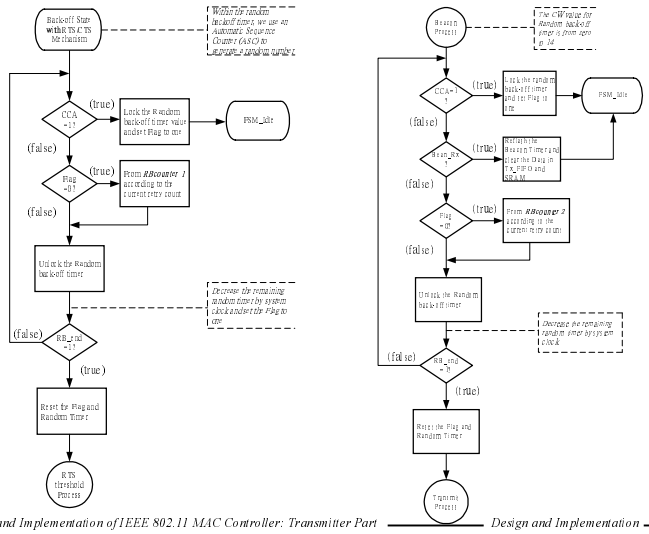


- Implement DCF features over *Ad Hoc* Network
  - CSMA/CA access scheme
  - Timeout scheme
  - RTS/CTS scheme
- Consist of Four parts:
  - Transmit FSM design
  - Transmit FIFO design
  - Receive FIFO design
  - Timer design

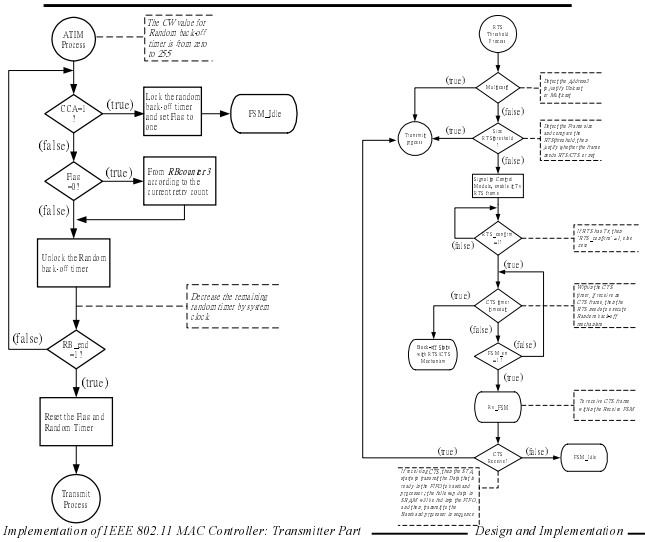
Transmission Finite State mechine Flow Chart



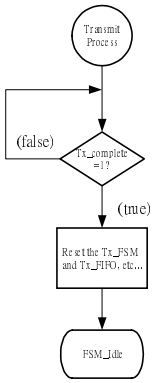
Transmission Finite State mechine Flow Chart (cont'd)



Transmission Finite State mechine Flow Chart (cont'd)



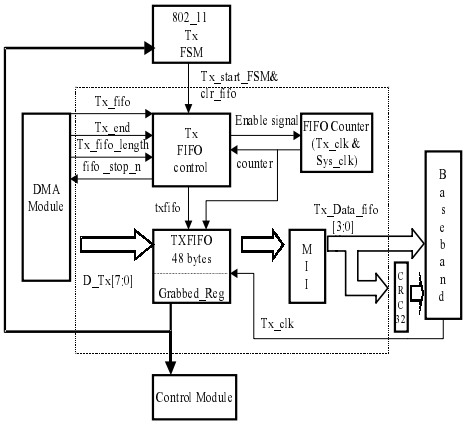
Transmission Finite State mechine Flow Chart (cont'd)



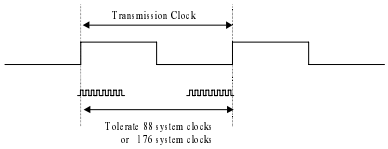
Special considerations of Transmission Finite State mechine

- Prioritize Retry frames within *Data Process*
  - ➢ *Retry frames directly invoking the Random back-off timer after ACKTimeout*
  - ➢ *Normal frames, after the expiration of DIFS, invoking Random back-off timer if the medium is idle following a busy medium.*
  - ➢ *Normal frames, after the expiration of DIFS, directly proceeding their transmission, if the medium is sensed idle for a period no less than DIFS.*
- RTS/CTS mechanism is launched only for the first fragment of an MSDU.
- A simple *Automatic Sequence Counter (ASC)* to generate random number

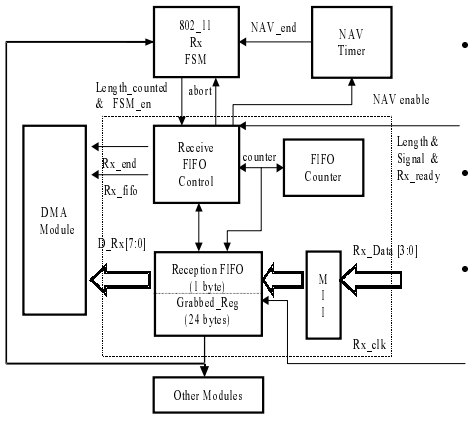
Transmit FIFO Design



- Contain *Controller*, *Counter*, and *Data path arbitrator* for Transmit FIFO
- DMA provides a *Tx_fifo signal* to transfer the 48-byte FIFO
- Grabbed Register to latch the PLCP Preamble and the MAC header



Receive FIFO Design

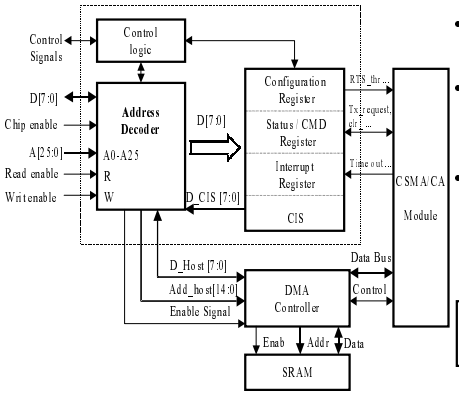


- Contain *Controller*, *counter*, and *Data path arbitrator* for Receive FIFO
- *one-byte* FIFO and *24-byte* Register
- FIFO counter counts based on the *Rx_clk*

Timers Design

- Random Back-off Timer
  - Contention window for data frame
    - CWmin - CWmax
  - Contention window for beacon frame
    - Zero - 2 * CWmin
  - Contention window for ATIM frame
    - Zero - Cwmax
- DIFS Timer
  - 40 us
- Slot Timer
  - 20 us
- ACK Timer
  - 10 us plus {112us for 1Mbps}
    or { 56us for 2 Mbps}
- CTS Timer
  - 2*10 us plus 2*20us plus
    {112us for 1Mbps}
    or { 56us for 2 Mbps}
- ATIM Timer
  - ATIM window (MIB) * Kus
- NAV Timer
  - (Rx_MAC_Header[31:16])
    * 44 for 1 Mbps and 2 Mbps

(2) Bus Interface Unit Module



- Support PCMCIA Spec Release 2.01
- Support the Attribute Memory
  - Configuration Registers
  - I/O Function
- Use the *Config registers* to control CSMA/CA module.