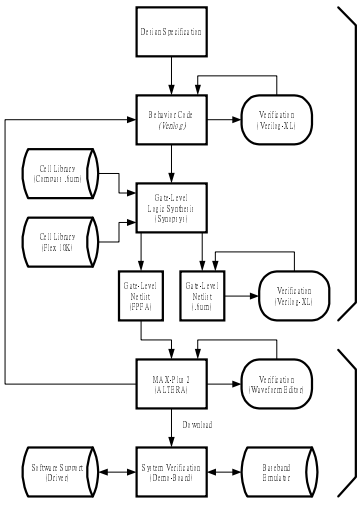
# 5. Verification and Simulation Results

- Design Flow
- Simulation Results
- Complexity Analysis





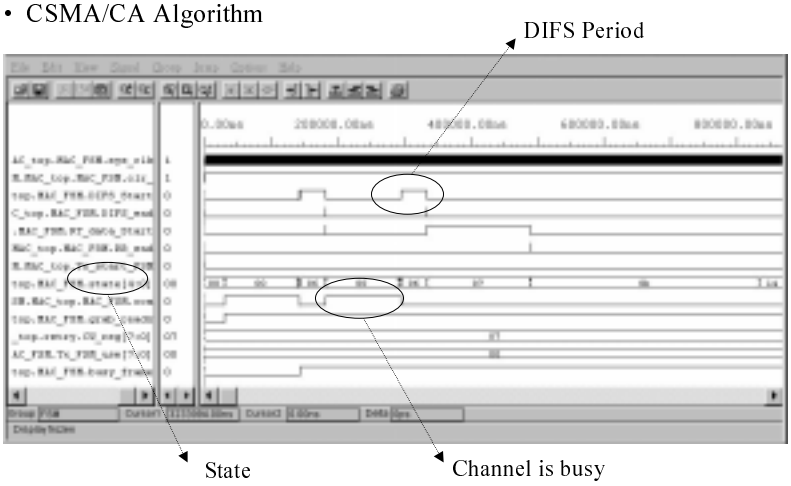
# Design Flow




- Separate the design flow to soft-verification ( behavior) and hard-verification (layout)
- Simulations
  - Behavior level (Verilog)
  - Gate level (Synopsys)
  - FPGA level (Altera)
- Verification
  - Combination of Driver and Baseband Emulator (ISA)

## Simulation Results

- CSMA/CA Algorithm

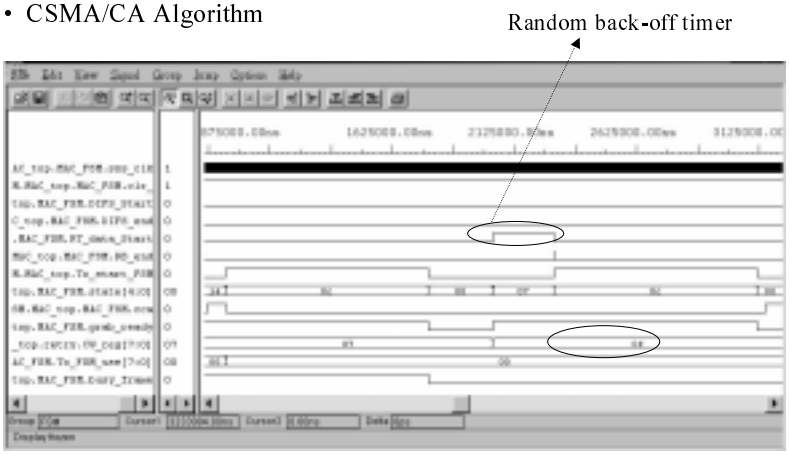







## Simulation Results (Cont'd)

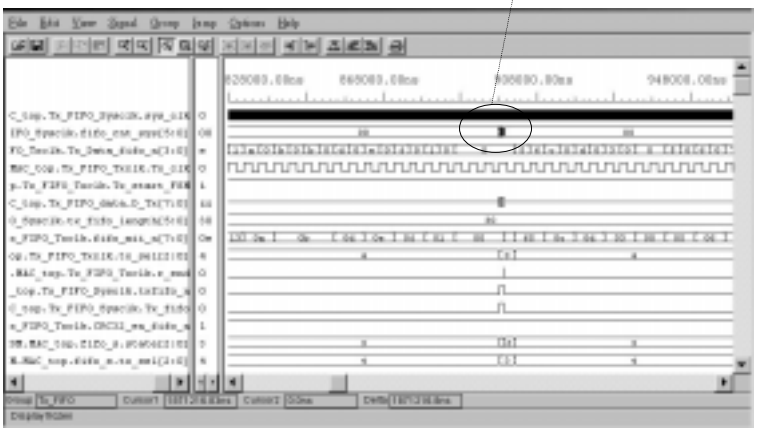
- CSMA/CA Algorithm



## Simulation Results (Cont'd)

- Transmit FIFO

Intercept Period



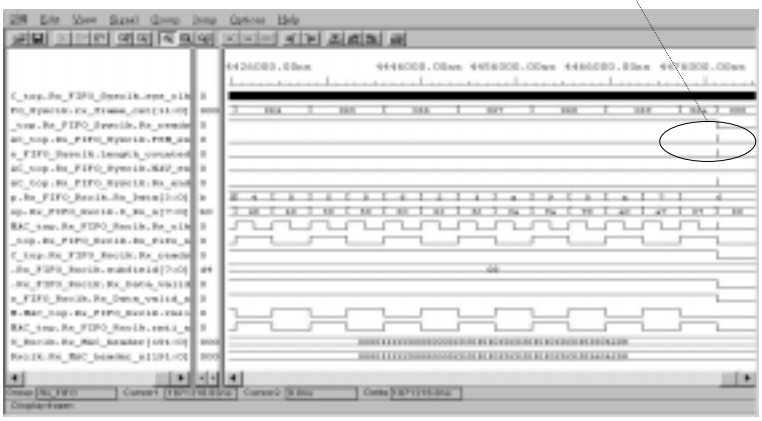




## Simulation Results (Cont'd)

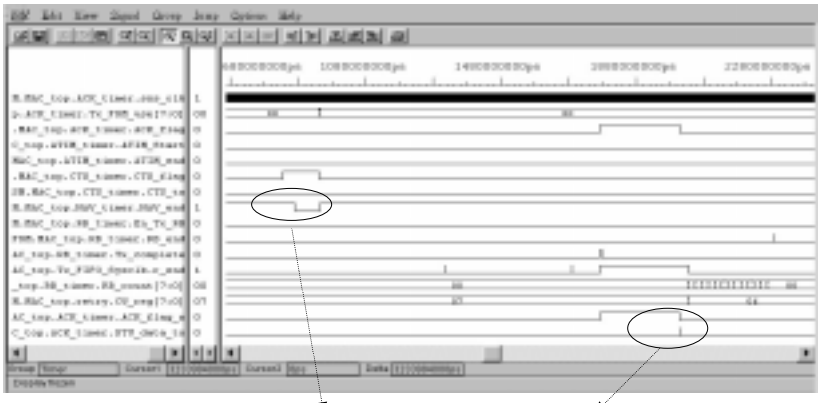
- Receive FIFO

Reception is over



## Simulation Results (Cont'd)

- Timer

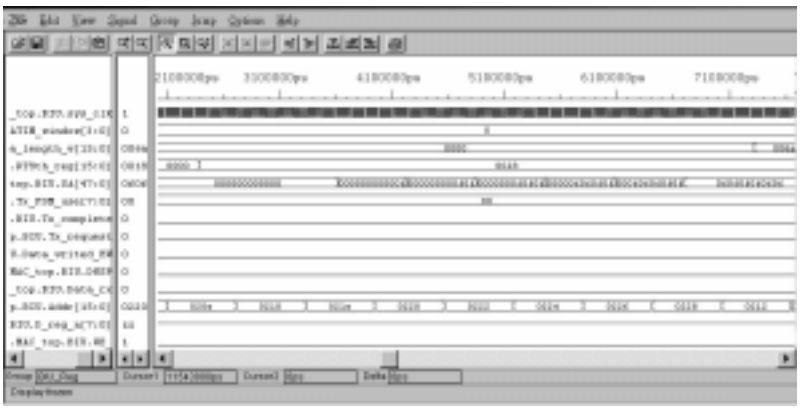






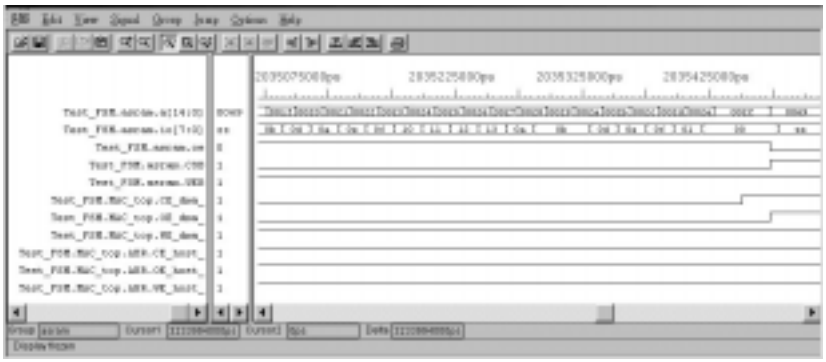

## Simulation Results (Cont'd)

- BIU module



## Simulation Results (Cont'd)

- SRAM interface (Read)







## Simulation Results (Cont'd)

- FPGA Simulation

## Complexity Anaylsis

- Gate counts (ASIC)
  - CSMA/CA module
    - *~ 14000 gates*
  - Bus Interface Module
    - *~ 3500 gates*
- Max endurable system timing
  - *20 ns* (Bottleneck is on the ASRAM write cycle) / 50MHz
- Testing over ALTERA FLEX10KA-2 FPGA
  - Pin count *240 pins (actual requirement 147pins and 5 testing pins)*
    - *79C30 144pins*
  - Flip/Flop 5932 (*actual requirement ~ 1500*)
  - Logic elements 4992 (*actual requirement ~ 4600*)